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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/782,717	CHOI, JOO S.	
	Examiner	Art Unit	
	Alexander Sofocleous	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) *18-55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-17* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/04, 3/05,4/05*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *12/8/2005* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on February 19, 2004, the Information Disclosure Statement filed on December 13, 2004, the Information Disclosure Statement filed on March 28, 2005, and the Information Disclosure Statement filed on April 20, 2005.

2. Claims 1-55 are pending in the case. Claims 1, 6, 11, 18, 23, 34, 44, 48, 50, 52, 54 are independent claims.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I. Claims 1-17, drawn to a device comprising a memory array and auxiliary circuit, classified in class 365, subclass 189.01. (Read/Write circuit)

Group II. Claims 18-22 and 44-47, drawn to a system comprising a memory array and controller and external terminals with accompanying method, classified in class 365, subclass 129. (Using particular element)

Group III. Claims 23-33, drawn to a method for transferring data, classified in class 710, subclass 1. (Input/Output data processing → input/output expansion)

Group IV. Claims 34-43, drawn to a method transferring groups of data to a memory array, classified in class 365, subclass 190. (Read/Write circuit → for complementary information)

Group V. Claims 48-55, drawn to a method for transferring groups of data on external terminals, classified in class 365, subclass 189.03. (Read/Write circuit → plural use of terminal)

Inventions Group II and Group I are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination does not require data lines. The subcombination has separate utility such as not requiring a controller.

Inventions Group III and Groups I,II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the method claims of Group III do not require a memory.

Inventions Group IV and Group I are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process.

(MPEP § 806.05(e)). In this case the apparatus claims of Group I do not require a first function to be applied to the data bits and a second function applied to the auxiliary bits.

Inventions Group V and Group II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the method claims of Group V do not require an auxiliary circuit.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Agent Viet Tong on December 8, 2005 at 12:48PM a provisional election was made without traverse to prosecute the invention of Group 1, claims 1-17. Affirmation of this election must be made by applicant in replying to this Office action. Claims 18-55 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Information Disclosure Statement

4. It is noted that there is a discrepancy on the 1449 filed on March 28, 2005 with the Patent Application Publication Number. Examiner assumes that the applicant intended to cite 2005/**00**28057 instead of 2005/**0**28057. Therefore, the examiner has

crossed through 2005/**0**28057 and not considered 2005/**0**28057 in favor of 2005/**00**28057, which has been cited on form PTO-892.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1, 6, 7, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Cypher (U.S. Patent 6,301,680 B1).**

Regarding independent claim 1, 6, and 11, Cypher '680 shows a device (Fig. 6 [700]) comprising a plurality of data lines (Fig. 6 [connections between 722, 720, and 710]) for transferring data and auxiliary information; a memory array (Fig. 6 [710]) for storing the data; an auxiliary circuit (Fig. 6 [722]) including a parity controller (Fig. 6 [722]) performing functions (in this case, parity checking; see column 8, lines 56-59 with respect to column 4, lines 64-66) on input/output data and having auxiliary lines (Fig. 6 [connection from 722 to 720 and 710]) carrying auxiliary information; and a transceiver

circuit (Fig. 6 [720]) connected to the memory array (Fig. 6 [710]) and the data lines (Fig. 6 [connection from 720 to 710]) for transferring data between the memory array (Fig. 6 [710]) and the data lines, the transceiver circuit (Fig. 6 [720]) also connects to the auxiliary circuit (Fig. 6 [722]) for transferring the auxiliary information between the auxiliary lines and the data lines.

Regarding dependent claim 7, Cypher '680 discloses that the check bits, or parity bits, are computed by an XOR, or comparison operation, of the data bits (column 5, lines 26-28).

7. **Claims 1, 6, 7, 8 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Cypher (U.S. Patent 6,304,992 B1).**

Regarding independent claim 1, 6, and 11, Cypher '992 shows a device (Fig. 7 [720]) comprising a plurality of data lines (not shown) for transferring data and auxiliary information; a memory array (Fig. 7 [702]) for storing the data; an auxiliary circuit (Fig. 7 [706]) including a parity controller (Fig. 7 [706]) performing functions (in this case, parity checking; see column 6, lines 29, 37-38, 50, 55-56) on input/output data and having auxiliary lines (not shown) carrying auxiliary information; and a transceiver circuit (Fig. 7 [708]) connected to the memory array (Fig. 7 [702]) and the data lines (not shown) for transferring data between the memory array (Fig. 7 [702]) and the data lines, the transceiver circuit (Fig. 7 [708]) also connects to the auxiliary circuit (Fig. 7 [706]) for transferring the auxiliary information between the auxiliary lines and the data lines.

Regarding dependent claim 7, Cypher '992 discloses that the check bits, or parity bits, or data bits, are compared (column 6, lines 29, 37-38, 50, 55-56).

Regarding dependent claim 8, Cypher '992 discloses that the check bits are stored which is indicative that the parity circuitry includes a storage unit (column 6, lines 38, 55-56).

8. **Claims 1-7,9, and 11-17 are rejected under 35 U.S.C. 102(a) or 35 U.S.C. 102(e) as being anticipated by Choi et al. (U.S. Patent Application 2005/0165999).**

The applied reference has a common assignee and a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding independent claim 1, Choi et al. show a device (Fig. 1 [100]) comprising a plurality of data lines (Fig. 1 [194]) for transferring data and auxiliary information; a memory array (Fig. 1 [102]) for storing the data; an auxiliary circuit (Fig. 1 [195]) having auxiliary lines (Fig. 1 [182, 184]) carrying auxiliary information; and a transceiver circuit (Fig. 1 [190]) connected to the memory array (Fig. 1 [102]) and the data lines (Fig. 1 [194]) for transferring data between the memory array (Fig. 1 [102]) and the data lines (Fig. 1 [194]), the transceiver circuit (Fig. 1 [190]) also connects to the

auxiliary circuit (Fig. 1 [195]) for transferring the auxiliary information between the auxiliary lines (Fig. 1 [182, 184]) and the data lines (Fig. 1 [194]).

Regarding dependent claim 2, Choi et al. show that the auxiliary circuit (Fig. 3 [195]) includes and inversion controller (Fig. 4; Fig. 3 [304]) connected to the transceiver circuit (Fig. 3 [190]) and the memory array (Fig. 1 [102]) for conditionally inverting the data (Fig. 4 [DI, Dout]).

Regarding dependent claim 3, Choi et al. show that the auxiliary circuit (Fig. 3 [195]) further includes a parity controller (Fig. 7 [307]) connected to the transceiver circuit (Fig. 3 [190]) and the memory array (Fig. 1 [102]) for generating a number of parity codes for the data (Fig. 7 [DI, Dout]).

Regarding dependent claim 4, Choi et al. show that the auxiliary circuit (Fig. 3 [195]) further includes a temperature reporting circuit (Fig. 3 [310]) connected to the transceiver circuit (Fig. 3 [190]) for generating temperature information of the device (paragraph 0133).

Regarding dependent claim 5, Choi et al. show that the auxiliary circuit (Fig. 3 [195]) further includes a calibrating circuit (Fig. 3 [313]) connected to the transceiver circuit (Fig. 3 [190]) for providing a time delay (paragraph 0149) based on the auxiliary information (Fig. 3 [CAL]; see paragraph 0147).

Regarding independent claim 6, Choi et al. show a device (Fig. 1 [100]) comprising a plurality of data lines (Fig. 1 [194]); a memory array (Fig. 1 [102]) for storing the data; an auxiliary circuit (Fig. 1 [195]) including a parity controller (Fig. 7 [307]) connected to the memory array (Fig. 1 [102]) for generating a plurality of parity

codes for the data; and a transceiver circuit (Fig. 7 [190]) connected to the memory array (Fig. 1 [102]) and the data lines (Fig. 1 [194]) for transferring data between the memory array (Fig. 1 [102]) and the data lines (Fig. 1 [194]), the transceiver circuit (Fig. 7 [190]) also connects to the parity controller circuit (Fig. 7 [307]) for transferring the parity codes between the parity controller (Fig. 7 [307]) and the data lines (Fig. 1 [194]).

Regarding dependent claim 7, Choi et al. show the parity controller includes a number of comparators (Fig. 7 [732]; in this case the "number" is 1) for comparing the bits of the data (paragraph 0118).

Regarding dependent claim 9, Choi et al. show the auxiliary circuit (Fig. 1 [195]) further includes an inversion controller (Fig. 3 [304]) connected to the transceiver circuit (Fig. 3 [190]) for conditionally inverting the data (Fig. 4 [DI, Dout]) transferred between the transceiver circuit (Fig. 3 [109]) and the memory array (Fig. 1 [102]).

Regarding independent claim 11, Choi et al. show a device (Fig. 1 [100]) comprising a plurality of data lines (Fig. 1 [194]); a memory array (Fig. 1 [102]) for storing input data and output data; an input auxiliary circuit (Fig. 1 [195]) configured for receiving input auxiliary information of the input data and configured for performing a function on the input data (Fig. 3 [DI]); an output auxiliary circuit (Fig. 1 [195]) configured for generating output auxiliary information of the output data and configured for performing a function on the output data (Fig. 3 [Dout]); and a transceiver circuit (Fig. 3 [190]) connected to the memory array (Fig. 1 [102]) and the data lines (Fig. 1 [194]) for transferring the input and output data (Fig. 3 [DI, Dout]) between the memory array (Fig. 1 [102]) and the data lines (Fig. 1 [194]), the transceiver circuit (Fig. 7 [190]) also

connects to the input and output auxiliary circuits (Fig. 1 [195]) for transferring the input and output auxiliary information between the input and output auxiliary circuits (Fig. 1 [195]) and data lines (Fig. 1 [194]).

Regarding dependent claim 12, Choi et al. show that the output auxiliary circuit (Fig. 3 [195]) includes an output inverting circuit (Fig. 3 [304]) for conditionally inverting the output data (Fig. 4 [Dout]) based on the output auxiliary information (Fig. 4 [INVo]; paragraph 0087).

Regarding dependent claim 13, Choi et al. show that the output auxiliary circuit (Fig. 3 [195]) further includes an output parity controller (Fig. 7 [307]) for generating a number of parity codes (Fig. 7 [Po]; in this case the "number" is 1) for the output data (Fig. 7 [Dout]; paragraph 0117).

Regarding dependent claim 14, Choi et al. show that the output auxiliary circuit (Fig. 3 [195]) further includes a temperature reporting circuit (Fig. 3 [310]) for generating temperature information of the device (paragraph 0133).

Regarding dependent claim 15, Choi et al. show that the input auxiliary circuit (Fig. 3 [195]) includes an input inverting circuit (Fig. 3 [304]) for conditionally inverting the input data (Fig. 4 [DI]) based on the output auxiliary information (Fig. 4 [INVi]; paragraph 0087).

Regarding dependent claim 16, Choi et al. show that the input auxiliary circuit (Fig. 3 [195]) further includes an input parity controller (Fig. 7 [307]) for generating a number of parity codes (Fig. 7 [Pii]; in this case the "number" is 1) for the input data (Fig. 7 [DI]; paragraph 0117).

Regarding dependent claim 17, Choi et al. show that the input auxiliary circuit (Fig. 3 [195]) further includes a calibrating circuit (Fig. 3 [313]) for providing a time delay (paragraph 0149) based on the input auxiliary information (Fig. 3 [CAL]; see paragraph 0147).

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. **Claims 1-5, 6, 7, 9, and 11-15 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 8-12 of copending Application No. 2005/0165999.** Although the conflicting claims are not identical, they are not patentably distinct from each other because both applications claim devices with a memory array, data paths, transceiver, and auxiliary

circuit with an inversion controller, a parity controller, a temperature reporter, and a timing calibrator.

Regarding independent claim 1 and 11, Choi et al.'s claim 8 recites all of the claim limitations with respect to the following explanations: input/output data path is plurality of data lines for transferring data, plurality of write/read strobe transceivers transfer auxiliary data, lines connected auxiliary circuit to data transceivers carry auxiliary information, and data transceiver circuit transfers data to data lines to memory.

Regarding dependent claim 2, and 12, Choi et al.'s claim 9 recites that the auxiliary circuit includes an inversion controller that conditionally inverts the output data. Choi et al,'s claim 8 establishes that auxiliary circuit is connected to the transceiver circuit.

Regarding dependent claim 3, and 13, Choi et al.'s claim 10 recites that the auxiliary circuit includes a parity controller for generating a parity code of the output data (in this case the "number of parity codes" is 1). Choi et al,'s claim 8 establishes that auxiliary circuit is connected to the transceiver circuit.

Regarding dependent claim 4 and 14, Choi et al.'s claim 11 recites that the auxiliary circuit includes a temperature reporter controller for generating temperature information of the device. Choi et al,'s claim 8 establishes that auxiliary circuit is connected to the transceiver circuit.

Regarding dependent claim 15, Choi et al.'s claim 9 also recites that the auxiliary circuit includes an inversion controller that conditionally inverts the input data.

Choi et al,'s claim 8 establishes that auxiliary circuit is connected to the transceiver circuit.

Regarding dependent claim 5, Choi et al.'s claim 12 recites that the auxiliary circuit includes a calibrator for calibrating timing information. Choi et al,'s claim 8 establishes that auxiliary circuit is connected to the transceiver circuit.

Regarding claims 6 and 9, Choi et al.'s claim 8, 9, and 10 recite all of the claim limitations with respect to the following explanations: input/output data path is plurality of data lines for transferring data, plurality of write/read strobe transceivers transfer auxiliary data, lines connected auxiliary circuit to data transceivers carry auxiliary information, and data transceiver circuit transfers data to data lines to memory, the auxiliary circuit includes an inversion controller that conditionally inverts the data, and the auxiliary circuit includes a parity controller for generating a parity code of the output data.

Regarding dependent claim 7, Choi et al.'s claim 62 recites all of the claim limitations for Applicant's claim 6 (from which Applicant's claim 7 depends) with respect to the following explanations: input/output data path is plurality of data lines, the parity controller is an auxiliary circuit, plurality of data transceivers transfer input/output data, and the data transceivers are connected to the parity controller. Choi et al.'s claims 63-65 establish the nature of the parity controller and that the parity controller includes a comparator (in this case the "number of comparators" is 1).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 10, the following is an examiner's statement of reasons for allowance: There is no teaching or suggestion in the prior art of a storage unit for the inversion controller included with the auxiliary circuit where the transceiver unit connects to the storage unit of the inversion controller for transferring the inverting codes between the inverting parity controller and the data lines.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Ooba et al. (U.S. Patent 4,794,597), and Hargan (U.S. Patent Application Publication 2005/0190635)

Ooba et al. show a memory unit connected to parity and inverting circuitry.

Hargan, which is a commonly assigned co-pending application, shows an array with transceivers and a conditioning circuit.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

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